

Lecture 1

Introduction

- **VLSI realization process**
- **Verification and test**
- **Ideal and real tests**
- **Costs of testing**
- **Roles of testing**
- **A modern VLSI device - system-on-a-chip**

VLSI Realization Process

Customer's need

Determine requirements

Write specifications

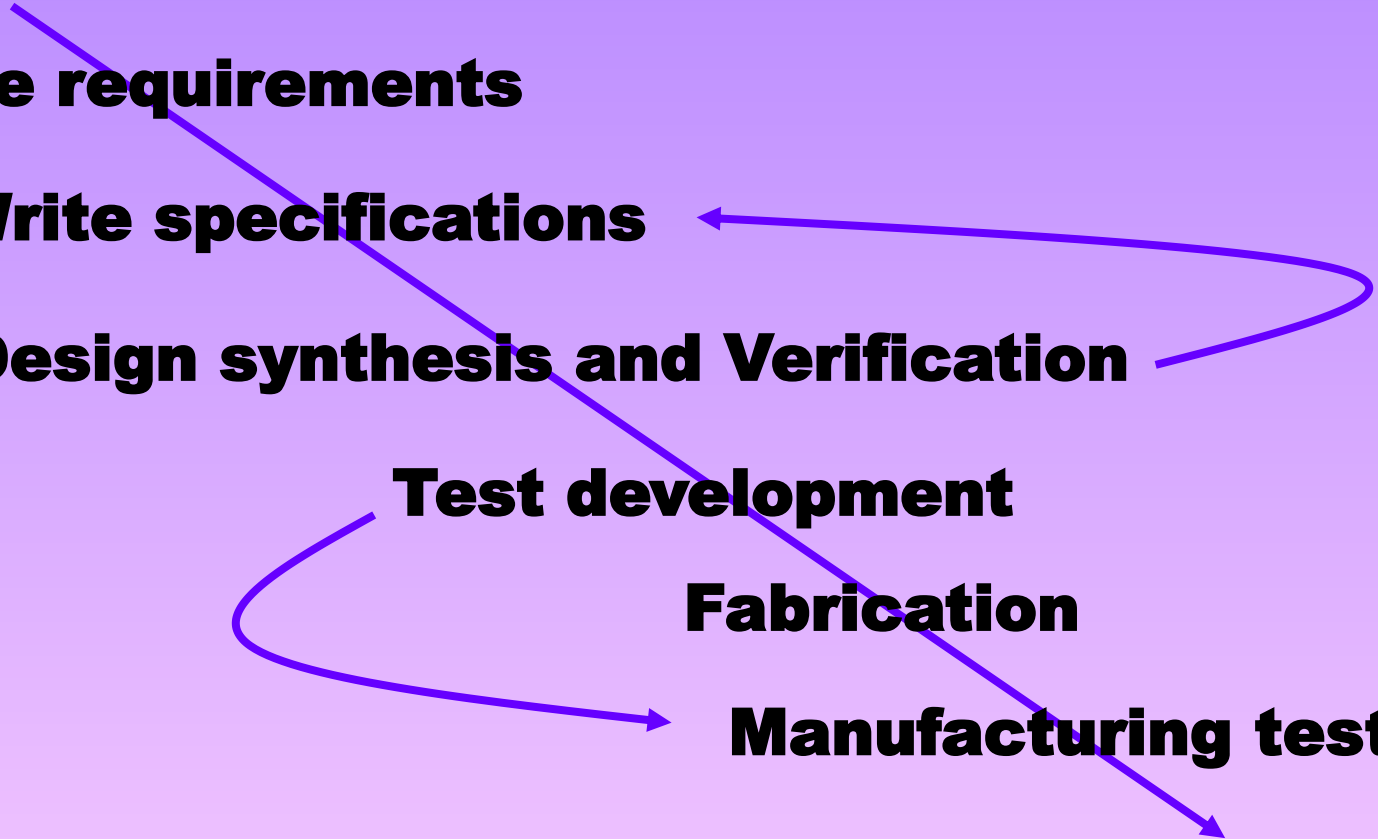
Design synthesis and Verification

Test development

Fabrication

Manufacturing test

Chips to customer



Definitions

- **Design synthesis:** Given an I/O function, develop a procedure to manufacture a device using known materials and processes.
- **Verification:** Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.
- **Test:** A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.

Verification vs. Test

- **Verifies correctness of design.**
 - **Performed by simulation, hardware emulation, or formal methods.**
 - **Performed once prior to manufacturing.**
 - **Responsible for quality of design.**
- **Verifies correctness of manufactured hardware.**
 - **Two-part process:**
 - 1. Test generation: software process executed once during design**
 - 2. Test application: electrical tests applied to hardware**
 - **Test application performed on every manufactured device.**
 - **Responsible for quality of devices.**

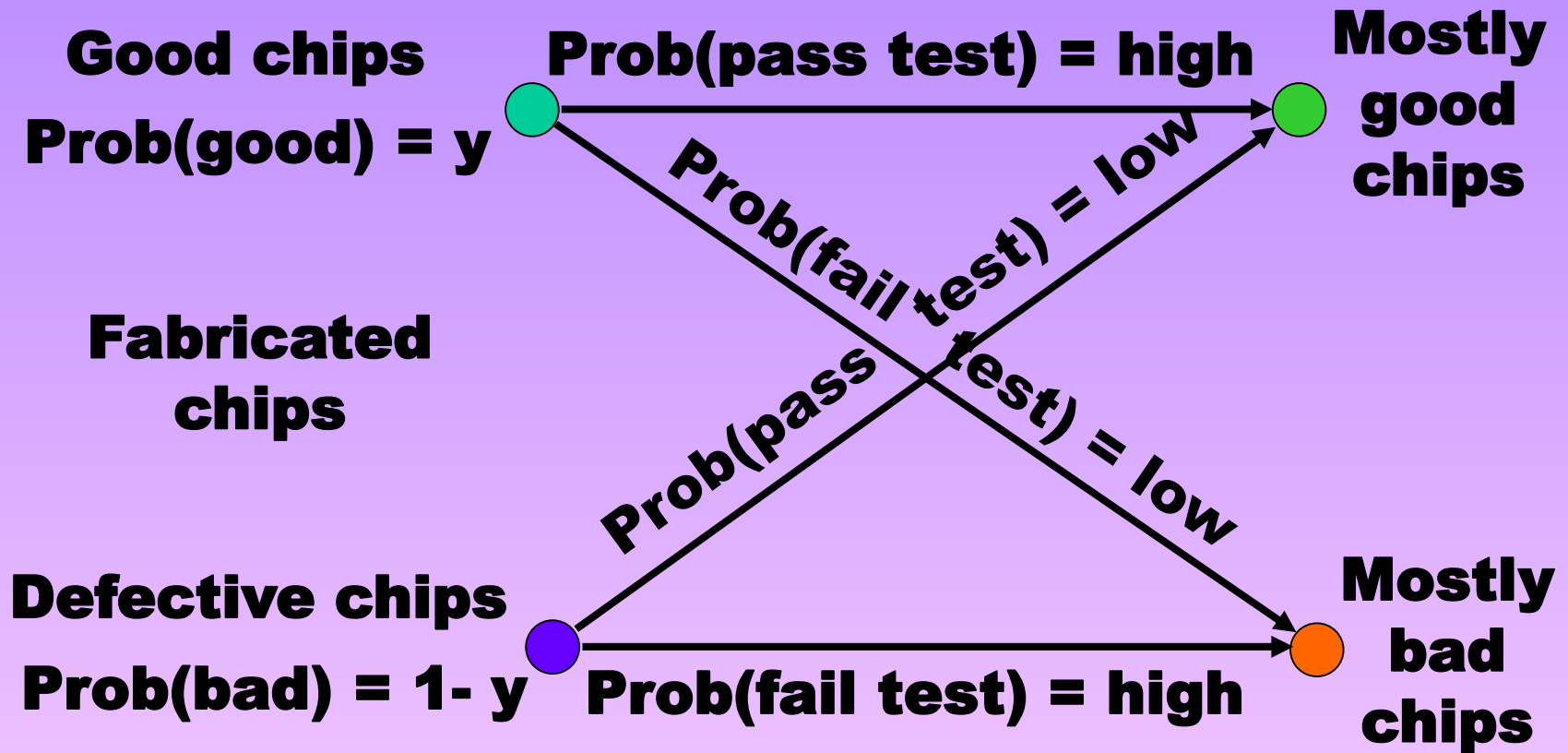
Problems of Ideal Tests

- **Ideal tests detect all defects produced in the manufacturing process.**
- **Ideal tests pass all functionally good devices.**
- **Very large numbers and varieties of possible defects need to be tested.**
- **Difficult to generate tests for some real defects. *Defect-oriented testing is an open problem.***

Real Tests

- **Based on analyzable fault models, which may not map on real defects.**
- **Incomplete coverage of modeled faults due to high complexity.**
- **Some good chips are rejected. The fraction (or percentage) of such chips is called the *yield loss*.**
- **Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the *defect level*.**

Testing as Filter Process



Costs of Testing

- ***Design for testability (DFT)***

 - Chip area overhead and yield reduction**

 - Performance overhead**

- **Software processes of test**

 - Test generation and fault simulation**

 - Test programming and debugging**

- **Manufacturing test**

 - Automatic test equipment (ATE)* capital cost**

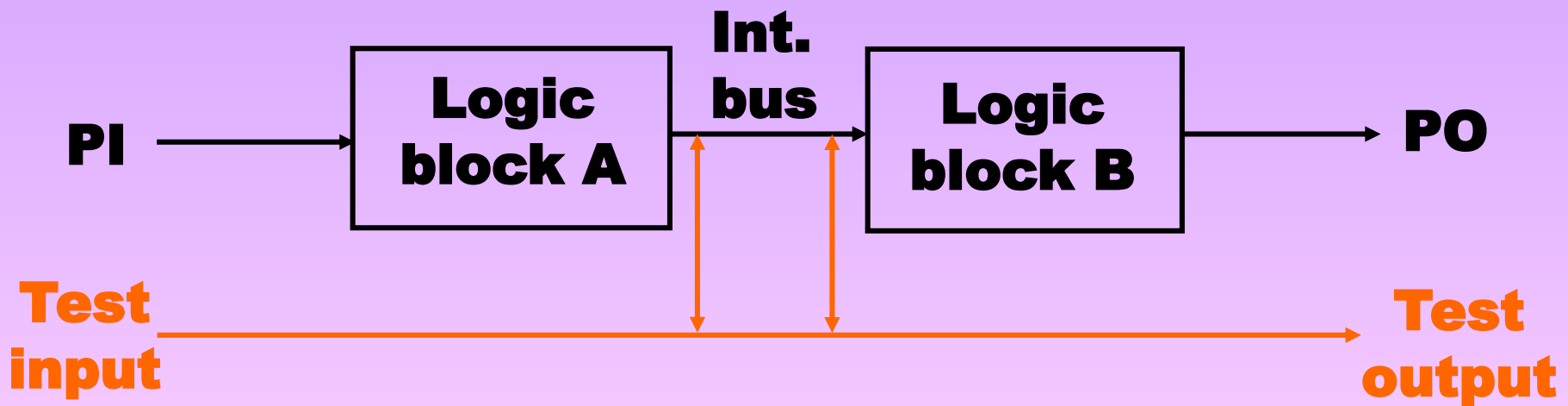
 - Test center operational cost**

Design for Testability (DFT)

DFT refers to hardware design styles or added hardware that reduces test generation complexity.

Motivation: Test generation complexity increases exponentially with the size of the circuit.

Example: Test hardware applies tests to blocks A and B and to internal bus; avoids test generation for combined A and B blocks.



Roles of Testing

- **Detection:** Determination whether or not the *device under test* (DUT) has some fault.
- **Diagnosis:** Identification of a specific fault that is present on DUT.
- **Device characterization:** Determination and correction of errors in design and/or test procedure.
- ***Failure mode analysis* (FMA):** Determination of manufacturing process errors that may have caused defects on the DUT.